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IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Please amend the claims as follows:

1. (Currently Amended) An evaluation method of a TFT comprising:

a step of forming a TAG and the TFT over a same substrate, each having a gate electrode which is formed to have a first conductive film over a semiconductor film and a second conductive film over the first conductive film, ~~which is formed to have~~ the semiconductor film having a low concentration impurity region overlapping the gate electrode,

a step of measuring resistance of the low concentration impurity region of the TEG, and

estimating an impurity concentration of the low concentration impurity region of the TFT by the resistance,

wherein etching is performed simultaneously on the gate electrode of the TEG and the gate electrode of the TFT,

wherein an edge of the first conductive film extends beyond an edge of the second conductive film, and

wherein a side edge portion of the semiconductor film is provided between the edge of the first conductive film and the edge of the second conductive film.

2. (Currently Amended) An evaluation method of a TFT comprising:

a step of forming a TEG and the TFT over a same substrate, each having a gate electrode that is laminated with a first conductive film and a second conductive film over a semiconductor film which has a low concentration impurity region overlapping the gate electrode,

a step of measuring resistance of the low concentration impurity region of the TEG, and estimating an impurity concentration of the low concentration impurity region of the TFT by the resistance,

wherein an edge of the first conductive film extends [[over]] beyond an edge of the second conductive film, and

wherein a side edge portion of the semiconductor film is provided between the edge of the first conductive film and the edge of the second conductive film.

3. (Previously Presented) The evaluation method of the TFT according to Claim 2, wherein the first conductive film is formed from a TaN film and the second conductive film is formed from a W film.

4. (Currently Amended) An evaluation method of a TFT comprising:

a step of forming a TEG and the TFT over a same substrate, each having a gate electrode with a taper which is formed to have a first conductive film over a semiconductor film and a second conductive film over the first conductive film, ~~which is formed to have~~ the semiconductor film having a low concentration impurity region overlapping the taper of the gate electrode,

a step of measuring resistance of the low concentration impurity region of the TEG, and

estimating an impurity concentration of the low concentration impurity region of the TFT in accordance with the taper by the resistance,

wherein the gate electrode with the taper is formed by taper etching, which is performed simultaneously on the gate electrode of the TEG and the gate electrode of the TFT,

wherein an edge of the first conductive film extends beyond an edge of the second conductive film, and

wherein a side edge portion of the semiconductor film is provided between the edge of the first conductive film and the edge of the second conductive film.

5. (Currently Amended) An evaluation method of a TFT comprising:

a step of forming a TEG and the TFT over a same substrate, each having a gate electrode that is laminated with a first conductive film and a second conductive film each having a taper over a semiconductor film which has a low concentration impurity region overlapping the taper of the gate electrode,

a step of measuring resistance of the low concentration impurity region of the TEG, and

estimating an impurity concentration of the low concentration impurity region of the TFT in accordance with the taper by the resistance,

wherein an edge of the first conductive film extends [[over]] beyond an edge of the second conductive film, and

wherein a side edge portion of the semiconductor film is provided between the edge of the first conductive film and the edge of the second conductive film.

6. (Previously Presented) The evaluation method of the TFT according to Claim 5, wherein the first conductive film having the taper is formed from a TaN film and the second conductive film having the taper is formed from a W film.

7. (Currently Amended) An evaluation method of a TFT comprising:

a step of forming a first TEG, a second TEG, a third TEG and the TFT over a same substrate, each having a gate electrode that is laminated with a first conductive film and a second conductive film over a semiconductor film which has a low concentration impurity region overlapping the gate electrode;

a step of measuring resistance of the low concentration impurity of the first TEG;

a step of measuring resistance of a channel forming region of the second TEG;

a step of measuring resistance of an impurity region of the third TEG; and

estimating impurity concentrations of the low concentration impurity region, a channel forming region and an impurity region in the TFT by the resistance,

wherein a side edge portion of the semiconductor film in the first TEG is provided between an edge of the first conductive film and an edge of the second conductive film,

wherein an edge of the second conductive film in the second TEG is extended [[over]] beyond a side edge portion of the semiconductor film, and

wherein an edge of the first conductive film in the third TEG is not extended [[over]] beyond a side edge portion of the semiconductor film.

8. (Previously Presented) The evaluation method of the TFT according to Claim 7, wherein a plurality of the first to the third TEGs are provided.

9. (Previously Presented) The evaluation method of the TFT according to Claim 7, wherein the first conductive film is formed from a TaN film and the second conductive film is formed from a W film.

10. (Previously Presented) The evaluation method of the TFT according to Claim 7, wherein edges of the first conductive film and the second conductive film have a taper.

11. (Previously Presented) The evaluation method of the TFT according to Claim 1, wherein in the TEG, a correlation of the resistance and an overlapping position of the first conductive film or the second conductive film and the semiconductor film is obtained.

12. (Previously Presented) The evaluation method of the TFT according to Claim 2, wherein in the TEG, a correlation of the resistance in the TEG and an overlapping position of the first conductive film or the second conductive film and the semiconductor film is obtained.

13. (Previously Presented) The evaluation method of the TFT according to Claim 4, wherein in the TEG, a correlation of the resistance in the TEG and an overlapping position of the first conductive film or the second conductive film and the semiconductor film is obtained.

14. (Previously Presented) The evaluation method of the TFT according to Claim 5, wherein a correlation of the resistance in the TEG and an overlapping position of the first conductive film or the second conductive film and the semiconductor film is obtained.

15. (Previously Presented) The evaluation method of the TFT according to Claim 7, wherein a correlation of the resistance in the TEG and an overlapping position of the first conductive film or the second conductive film and the semiconductor film is obtained.

16. (Previously Presented) The evaluation method of the TFT according to Claim 1, wherein the TEG has a test element for measuring resistance of the low concentration impurity region.

17. (Previously Presented) The evaluation method of the TFT according to Claim 2, wherein the TEG has a test element for measuring resistance of the low concentration impurity region.

18. (Previously Presented) The evaluation method of the TFT according to Claim 4, wherein the TEG has a test element for measuring resistance of the low concentration impurity region.

19. (Previously Presented) The evaluation method of the TFT according to Claim 5, wherein the TEG has a test element for measuring resistance of the low concentration impurity region.

20. (Previously Presented) The evaluation method of the TFT according to Claim 7, wherein the TEG has a test element for measuring resistance of the low concentration impurity region.

21. (Original) A method of manufacturing a semiconductor device characterized by having a TFT manufactured by using the evaluation method as recited in Claim 1.

22. (Original) A method of manufacturing a semiconductor device characterized by having a TFT manufactured by using the evaluation method as recited in Claim 2.

23. (Original) A method of manufacturing a semiconductor device characterized by having a TFT manufactured by using the evaluation method as recited in Claim 4.

24. (Original) A method of manufacturing a semiconductor device characterized by having a TFT manufactured by using the evaluation method as recited in Claim 5.

25. (Original) A method of manufacturing a semiconductor device characterized by having a TFT manufactured by using the evaluation method as recited in Claim 7.

26. (Withdrawn) A method of manufacturing a semiconductor device including a TFT including a semiconductor film having an impurity region formed over an insulating substrate, and a gate electrode formed over the semiconductor film by using a mask, characterized by forming a TEG having impurity regions in a plurality of regions on the insulating substrate, calculating misalignment of a mask of the TEG before and/or after an activation step of the TFT, and calculating shrinkage or expansion of the substrate by the calculated misalignment of the mask.

27. (Withdrawn) A method of manufacturing a semiconductor device including a TFT including a semiconductor film having a low concentration impurity region and a high concentration impurity region formed over an insulating substrate, and a gate electrode formed over the semiconductor film by using a mask so as to overlap the low concentration impurity region, characterized by forming a TEG having a low concentration impurity region and a high concentration impurity region in a plurality of regions on the insulating substrate, calculating misalignment of a mask of the TEG before and/or after an activation step of the TFT, and calculating shrinkage or expansion of the substrate by the calculated misalignment of the mask.

28. (Withdrawn) An article characterized in that a TEG and a TFT over a same substrate, having a gate electrode over a semiconductor film which is formed so as to have a low concentration impurity region overlapping the gate electrode.

29. (Withdrawn) An article characterized in that a TEG and a TFT over a same substrate, having a gate electrode laminated with a first conductive film and a second conductive film over a semiconductor film which has a low concentration impurity region overlapping the gate electrode, wherein an edge of the first conductive film extends over an edge of the second conductive film, wherein a side edge portion of the semiconductor film is provided between the edge of the first conductive film and the edge of the second conductive film.

30. (Withdrawn) The article according to Claim 29, characterized in that the first conductive film is formed from a TaN film and the second conductive film is formed from a W film.

31. (Withdrawn) The article according to Claim 28 characterized by including a gate electrode having a taper over a semiconductor film which has a low concentration impurity region overlapping the gate electrode.

32. (Withdrawn) The article according to Claim 29 characterized by including a gate electrode having a taper over a semiconductor film which has a low concentration impurity region overlapping the gate electrode.

33. (Withdrawn) A program for controlling a dosage for operating a computer that controls a quantity of impurities to be added of a TFT provided over a same substrate as a TEG as operation means for obtaining a resistance distribution of the TEG, as means for memorizing a manufacturing condition of a TFT or a design condition of a device, as means for judging an quantity of impurities to be added based on the means for memorizing, and as means for setting a doping apparatus of quantity of impurities that is obtained from the means for memorizing.

34. (Withdrawn) A program for controlling a dosage for operating a computer that controls a quantity of impurities to be added of a TFT that has a gate electrode formed by using a mask and that is provided over a same substrate as a TEG as operation means for obtaining a resistance distribution of the TEG by making operation of a misalignment of the mask, as means for memorizing a manufacturing condition of a TFT or a design condition of a device, as means for judging an quantity of impurities to be added based on the means for memorizing, and as means for setting a doping apparatus of quantity of impurities that is obtained from the means for memorizing.

35. (Withdrawn) A computer-readable recording medium that records a program for controlling dosage for operating a computer that controls a quantity of impurities to be added of a TFT provided over a same substrate as a TEG as operation means for obtaining a resistance distribution of the TEG, as means for memorizing a manufacturing condition of a TFT or a design condition of a device, as means for judging an quantity of impurities to be added based on the means for memorizing, and as means for setting a doping apparatus of quantity of impurities that is obtained from the means for memorizing.

36. (Withdrawn) A computer-readable recording medium that records a program for controlling dosage for operating a computer that controls a quantity of impurities to be added of a TFT that has a gate electrode formed by using a mask and that is provided over a same substrate as a TEG as operation means for obtaining a resistance distribution of the TEG by making operation of a misalignment of the mask, as means for memorizing a manufacturing condition of a TFT or a design condition of a device, as means for judging an quantity of impurities to be added based on the means for memorizing, and as means for setting a doping apparatus of quantity of impurities that is obtained from the means for memorizing.

37. (New) The evaluation method of the TFT according to Claim 1, wherein the low concentration impurity region is provided between a channel forming region and a source region or drain region in the semiconductor film.

38. (New) The evaluation method of the TFT according to Claim 2, wherein the low concentration impurity region is provided between a channel forming region and a source region or drain region in the semiconductor film.

39. (New) The evaluation method of the TFT according to Claim 4, wherein the low concentration impurity region is provided between a channel forming region and a source region or drain region in the semiconductor film.

40. (New) The evaluation method of the TFT according to Claim 5, wherein the low concentration impurity region is provided between a channel forming region and a source region or drain region in the semiconductor film.

41. (New) The evaluation method of the TFT according to Claim 7, wherein the low concentration impurity region is provided between the channel forming region and the impurity region.